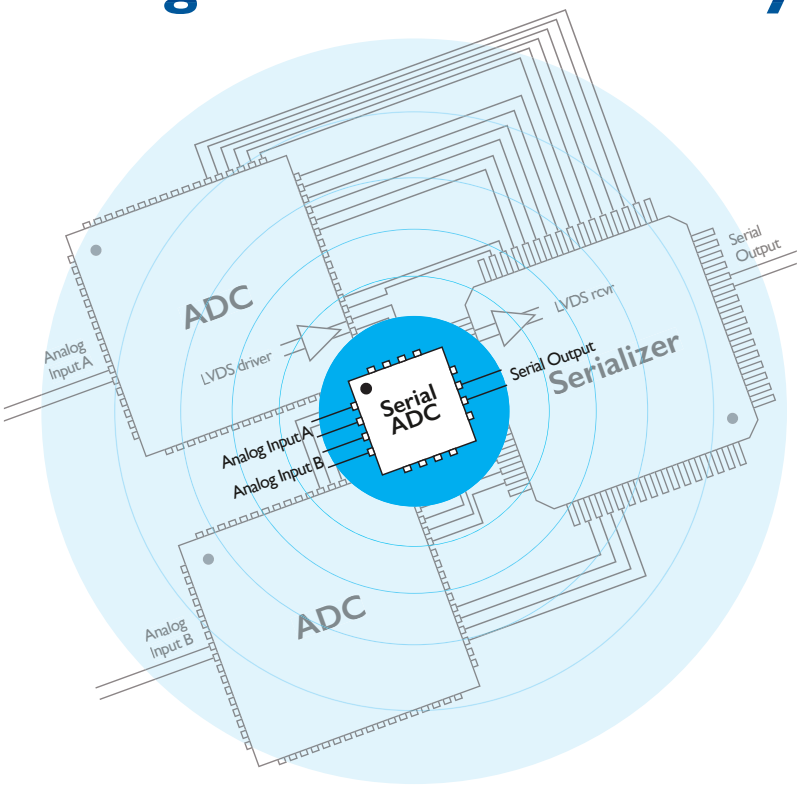
Central Development Laboratory

Serial Analog to Digital Converter ASIC

NRAO TECH TRANSFER

90% Less Power Consumption • 90% Smaller • Single-lane Fiber-ready Data Stream



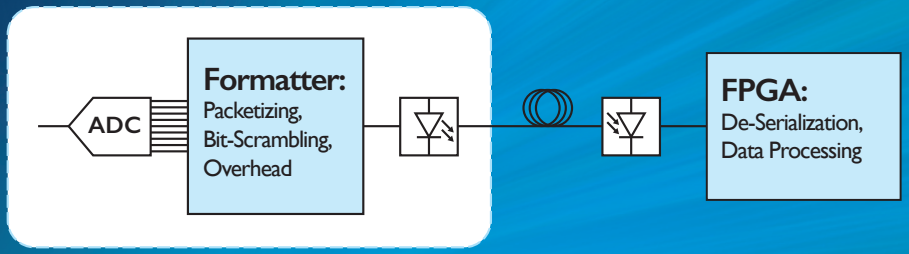
Why it matters...

- Ultra-low power consumption (333 mW for 20 Gbps, i.e. 2 channels of 10 Gbps @ 166 mW each)
- Tiny 5 mm QFN on transmit side of data link
- Allows for ultra-compact, wearable or hand-held, battery-operated sensors/collectors
- No need for co-locating DSP function at sensor
- Suitable for long distances over fiber, e.g. 80 km
- Implementable using either wired or wireless links
- Novel deserialization algorithm leverages the known statistics of natural signals to parse the bit stream after transmission

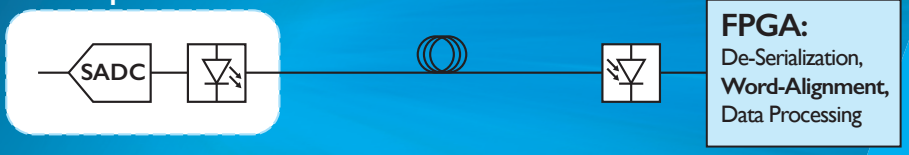
Second Generation ASIC Serial ADC

- ADC serial rate = 56 Gbps
- Resolution (dynamic) = 4-12 bits
- Sample rate:
  14 GS/s @ 4 bits
  7 GS/s @ 8 bits
  4.6 GS/s @ 12 bits
- Analog Input BW = 10.5 GHz
- Power dissipation = <500 mW
- Footprint = 6 mm QFN

Conventional Front-End



New Improved NRAO ASIC Front-End



Novel unformatted link reduces front-end overhead!

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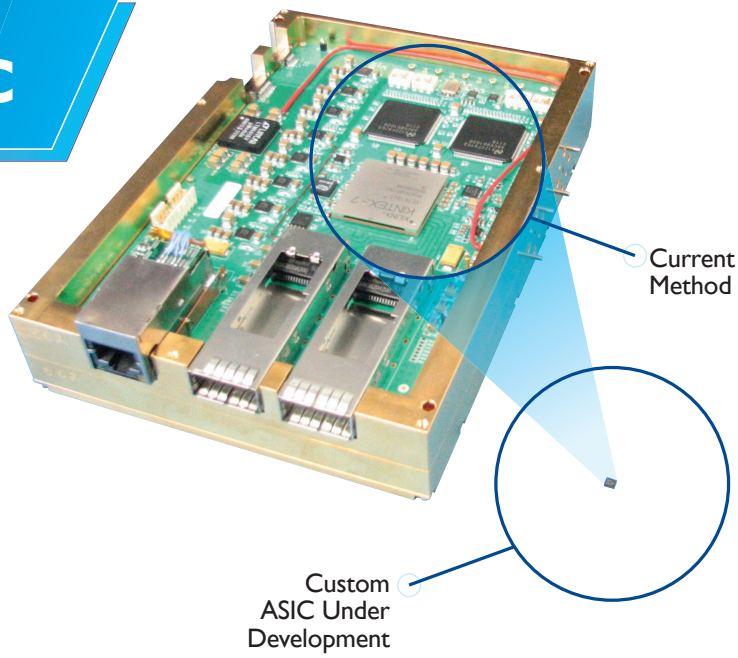

Key Milestones

- Technology Readiness Level (TRL) 6 - Aug 2018
- 10 Gbps proof-of-concept demonstrator built and tested 2016-2017
- In Development – ASIC design/build 2018-2019 suitable for 80+ km transmission via QSFP
- USPTO patent 8,688,617 – Apr 2014
- ECCN EAR99 – Ref. CJ 0316-17

First Generation Custom ASIC

- 333 mW, dual (2) channel ASIC, 5 mm QFN package
- 20 Gbps (10 Gbps per channel)
- 1.25 GS/s @ 8 bits resolution (per channel)
- No frame sync necessary
- Interface directly with industry-standard fiber-optic transceivers, e.g. QSFP+

Second Generation Custom ASIC

- Quad (4) channel ASIC, 6 mm QFN package
- 224 Gbps (56 Gbps per channel)
- 7 GS/s @ 8 bits resolution (per channel)
- No frame sync necessary
- Interface directly with industry-standard fiber-optic transceivers, e.g. QSFP+
- NRAO ngVLA development underway

ngvla
Next Generation Very Large Array

The Inventor

The inventor of the SADC, Matthew A. Morgan, PhD, is a Research Scientist at the National Radio Astronomy Observatory's Central Development Lab. He leads the Integrated Receiver Development (IRD) program, working on the design and development of new low noise receivers, components, and concepts for cm-wave, mm-wave, and submm-wave frequency ranges. Dr. Morgan has authored over 60 papers and holds seven patents in the areas of MMIC design, mm-wave system integration, high frequency packaging techniques, and reflectionless filters.

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