Central Development Laboratory

Scalable Radar Image Processing

NRAO TECH TRANSFER

Scalable Radar Image Processing Integrated Circuit with Enhanced Assurance

Most-advanced radar sensors use antenna arrays and wideband waveforms that are mostly processed in the digital domain. Currently, the required DSP solution must be designed ad hoc, based on either FPGAs or ASICs, which significantly increases the development cost. Our proposal consists of developing a "general purpose" integrated circuit to perform two basic DSP tasks required by these complex systems: beamforming and frequency channelization. A key specification of the proposed IC is that it can be replicated as many times as needed to satisfy the requirements of any application.

The proposed IC concept intends to exploit scale economies to decrease the costs of designing, developing and procuring advanced radar imaging processors. Only a "general-purpose" beamformer and frequency channelizer scalable and reconfigurable for an ample range of applications can benefit from scale economies. The pursued goal is to develop a COTS IC with minimal SWaP specifications, widely outperforming what current FPGA technology can achieve, and at a much lower cost than what developing an ASIC tailored to every single system would require. An additional benefit will be a significant decrease of the product's time to market. The IC will implement encryption and/or authentication features within the control interface for trusted communications.

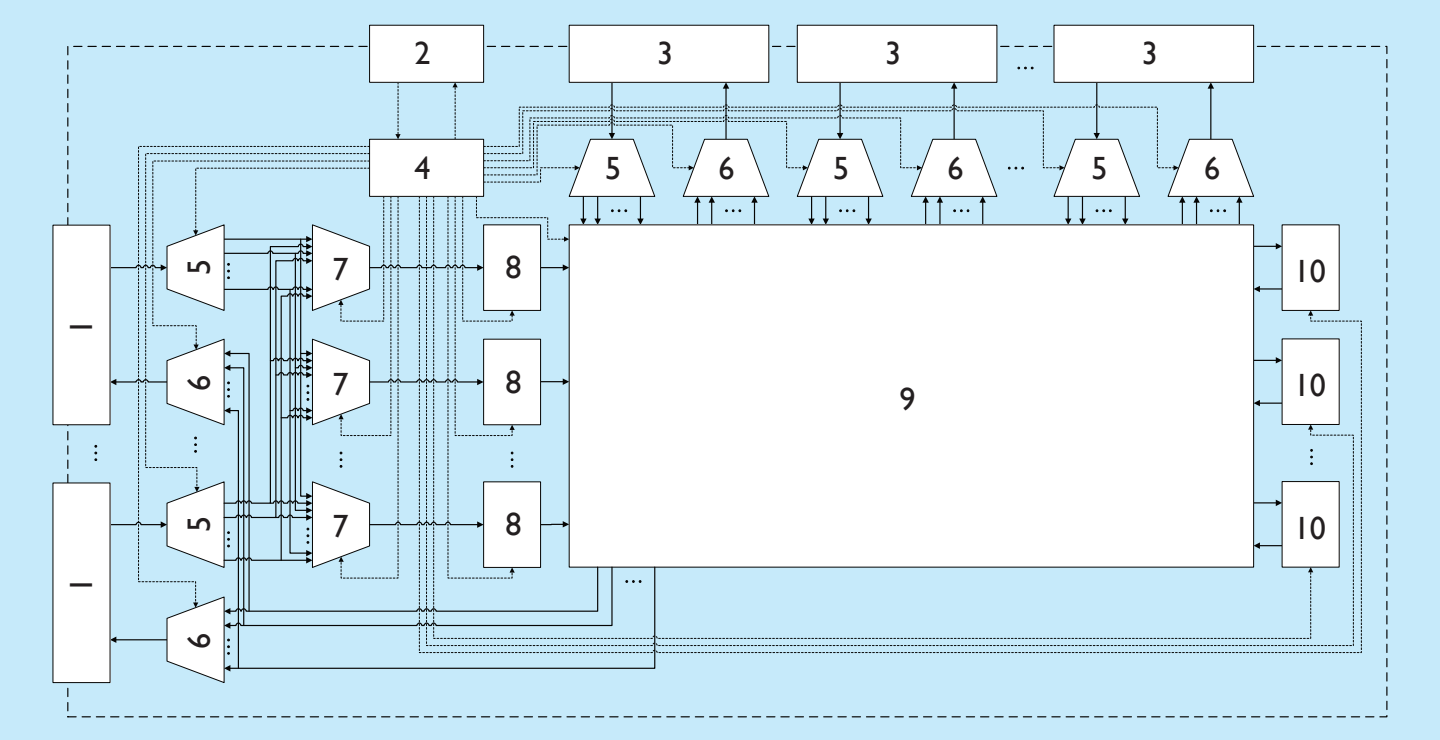
Thanks to its flexibility and its on-the-fly reconfigurability, the proposed IC can be utilized in an ample variety of applications. The ultimate goal is to make it available as a COTS component to help the industry reducing development and production costs. A secure version of the IC will provide its control interface with enhanced assurance by enabling encryption and authentication features for trusted communications.

Applications

- Electronically Scanned SAR
- UAV / Satellite
- Low SWAP
- Autonomous Products
- Beamforming
- 5G / IoT
- Through-the-wall Vision
- Biomedical Scanners
- Sonar Imaging

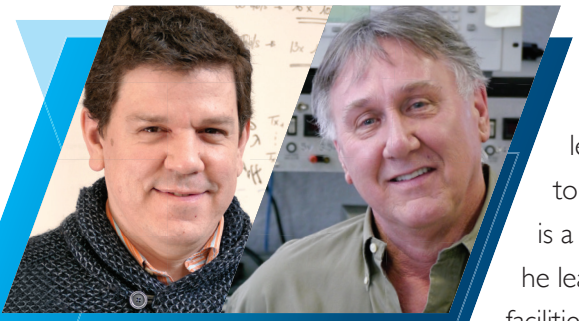
Scalable Radar Image Processing

SRIP Core Block Diagram



1. Input/output Interface
2. Control Interface
3. Beamforming Data interface
4. Configuration and Control
5. Deserializer
6. Serializer
7. Selector
8. Delay and Phase Correction
9. Linear Combination and Routing Logic
10. Frequency Channelizer

The Inventors



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